

VLSI Lab Tutorial 3

Virtuoso Layout Editing Introduction

1.0 Introduction

The purpose of this lab tutorial is to guide you through the design process in creating a custom IC layout for your CMOS inverter design. The layout represents masks used in wafer fabs to fabricate a die on a silicon wafer, which then eventually are packaged to become integrated circuit chips.

Upon completion of this tutorial, you should be able to:

- Create a mask layout of the CMOS inverter that you have designed earlier.
- Check that your layout satisfies the design rules of a 0.18 micron process technology using DRC.
- Extract a netlist including parasitic resistances and capacitances from the layout.
- Check that your layout passes the automatic verification against the inverter schematic created earlier.
- .
- More information can be found in the online documentation under the Custom IC and Deep Submicron Design category. Under Custom IC Layout, there is the Layout section that you may find helpful.

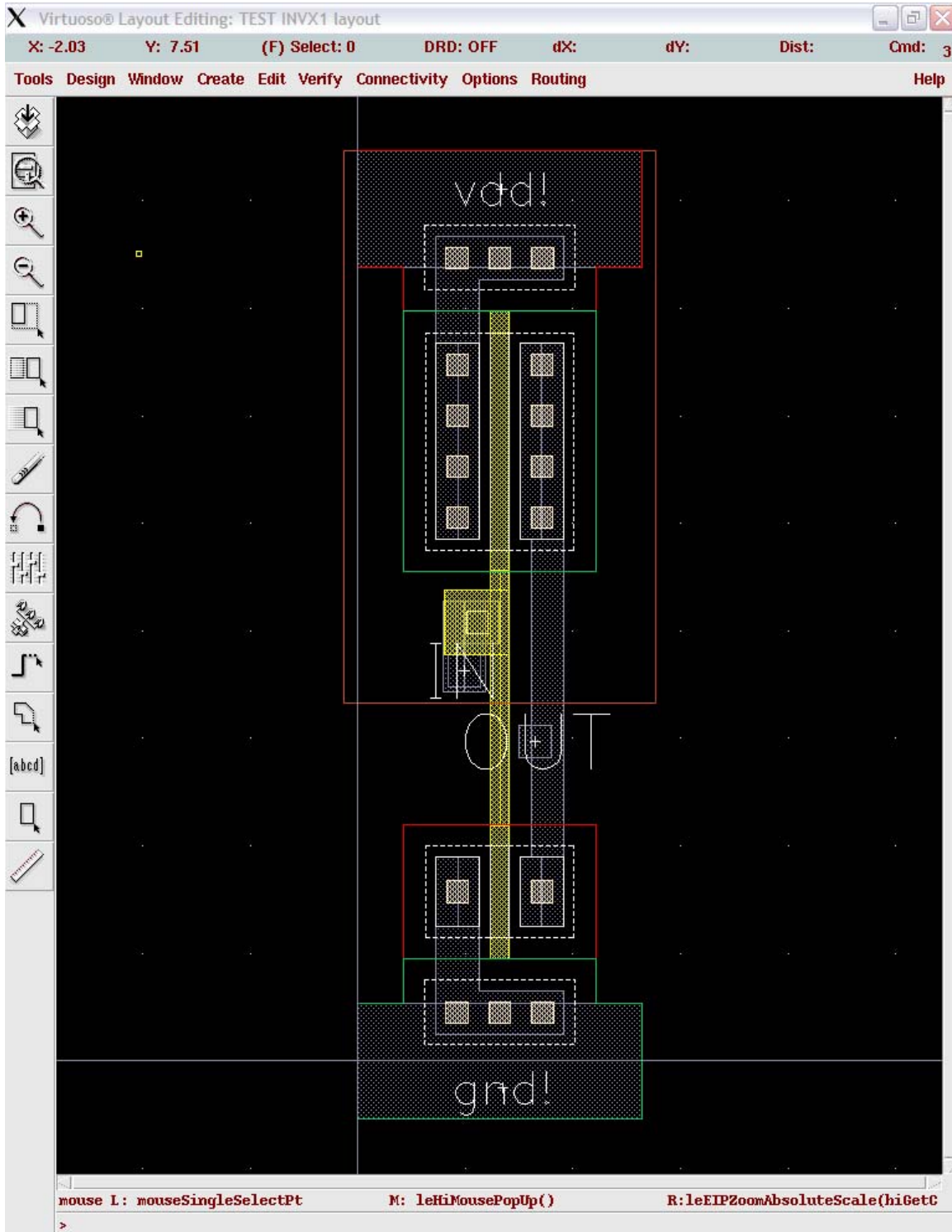
2.0 Inverter Layout Overview

The pictures on the facing page present an inverter layout very similar to the one you are about to create. The only significant difference should be the transistor widths. The inverter you create should have transistor widths matching the values you determined in the tutorial 1.

This layout is in the style of standard cells used for automated placement and routing of random logic. This does not, however, mean that this style of layout is bad for custom layout. It has some very useful features. In particular,

- It is designed so that the multiple instances of the cell can be connected together by abutment (i.e., placed immediately to the left and right of each other). The power, ground, input and output connections line up and will be connected.
- The layout lends itself to a left to right signal flow in the metal layer (used for the input and output) as well as vertical signal flow for short distances in polysilicon.

- If other types of logic cells have the same layout spacing between power and ground, then cells of various types can be chained together easily.



2.1 Design Rules

- Design rules are a set of rules (usually supplied by the manufacturer) that specify a minimum size or spacing requirements between the layers of the same type or of different types. This provides a safety margin for various process variations, to ensure that your design will still have reasonable performance after your circuit is fabricated.
- Note that the technology file you specified in the first tutorial (gpdk) defines the design rules that will be used to check your design. It also defines how the drawing layers are translated into masks for the IC. The design rule file used is **divaDRC.rul**.
- The following section will discuss about more common design rules.

2.2 Mask Layers

The mask layers are the various layers shown in the above diagram and are used to define the location and size of the devices and nets. Each layer can be treated as an individual layer meaning that two different layers have no electrical connection between them even though they happen to overlap. The layers are typically in different colors and shading (displayed in the layer selection window (LSW)-refer to section 3.2) and are defined by the **display.drf** file. If the layers display the same color, you need the **display.drf** file. The file **display.drf** can be found in *packages/cadence/cells/generic/gpdk_MIET_2.0*. copy this file to your Cadence running directory using the following command and exit and run icfb again:

```
cp /packages/cadence/cells/generic/gpdk_MIET_2.0/display.drf ./
```

Diffusion areas for source, drain and substrate contacts

- Rectangles on the **active** layer are used to define the region where doping is to be applied to the substrate (except under the polysilicon gate) to form the source and the drain of each transistor. For an NMOS transistor, the doping will be n+. For a PMOS transistor, this doping will be p+. It will be shown later how the type of doping is actually specified.
- Rectangles on the **poly** layer are used to define the strips of polysilicon used to form the gate of each transistor and to provide short distance connections between transistors in the inverter.

- The intersection of an **active** and **poly** region defines the channel of a transistor. Since the minimum size of active is 0.40μ and poly is 0.18μ , this means that the minimum transistor width must be 0.40μ and the minimum length must be 0.18μ .
- Note that in some cases, it may not be possible to draw an **active** area as a simple rectangle. The area may have to be one width at the source and drain to accommodate the required clearance around the source and drain contacts. It then may need to be notched to obtain the necessary transistor width for the intersection with **poly**.
- The **active** layer is also used to define regions that must be doped to allow a substrate or well contact. In p- substrate, the doping must be p+ type. In an N-well (where PMOS transistors are placed), the doping must be n+ type.
- Rectangles on the **nplus** and **pplus** layers are used to control the type of dopant applied to each diffusion area.

*Note: in gpdk technology, **active** layer is called **oxide**, **nplus** is called **Nimp**, and **pplus** is called **Pimp**. These are the layer names you will find in the LSW window (3.2).

2.3 N-well Regions

- PMOS transistors must be located in substrate with N type doping. In an N-well process, the substrate for the PMOS transistors is formed by diffusing N-type dopant into regions of the normally p-type substrate. Rectangles in the **nwell** layer, define these regions in which PMOS transistors can be placed.

2.4 Contacts

- $0.20u \times 0.20u$ squares drawn on the **contact** layer will cause metal plugs to be source, drain, and substrate or well contacts.
- $0.20u \times 0.20u$ squares drawn on the **contact** layer will cause the metal plugs to be placed into contact with the **poly** areas to form poly contacts.
- Metal placed on layer **metal1** will connect with these contacts.

2.5 Metal power ground and signal routing layers

- Rectangles on the **metal1** layer define regions of aluminum to be placed in the first metal layer. In this case metal1 is used for all inputs and outputs to the inverter.
- A $0.20\mu \times 0.20\mu$ square on **contact** provides a metal plug to connect routing on layer **metal1** to polysilicon routing below on the **poly** layer.

- In the 0.18 μ gpdk process, there are several other metal layers available (**metal2**, **metal3**, and so on). We are not going to use in this layout since it is not needed. However, in larger more complex layouts, both layers will be needed. Often it is a wise practice to route all signals horizontally on one layer and vertically on another layer.
- To connect the **metal1** layer to the **metal2** layer, a square on **via1** is used.
- You can connect other metal layers together using the appropriate via layers. For example, to connect the **metal2** layer to the **metal3** layer, a square on **via2** is used.

3.0 Virtuoso Layout Editing

- To start the Virtuoso Layout Editor, we need to create a new cellview from the library manager. In the new window that appears, set **Library Name** to **Tutorial** and type in **inverter** as the **Cell Name**. In the **View Name** field, type in the **layout** and press the **tab** key. The **Tool** field should change to **Virtuoso**. Click **OK** to continue.
- Two windows will appear. One is called the **Layer Selection Window (LSW)**. The LSW allows you to choose the layer on which you create objects, set which layers are selectable and set layer visibility. Note that the technology file that you entered in the first tutorial (**gpdk**) defines the layers and colors that will be available to you in the LSW.
- The other window is the layout window (**Virtuoso Layout Editing**) where you perform the place and the route of the inverter layout.



3.1 Setting up the Environment

Before you start doing your layout, you need to setup the grid size of the cellview so that each grid will correspond to a dimension that will make the layout process easier and allow for a more compact design.

- To set up a display environment, select **Options** → **Display**. The Display Option window will appear. In the window, change Minor Spacing to 0.1 and Major Spacing to 0.1. Change both X Snap Spacing and Y Snap Spacing to 0.01. The Spacing can be changed according to your requirement.
- Leave the other settings at their default setting. However, take note that those options will allow you to change the display of the cellview if need arises. Please refer to the online documentation if you need further information.
- The settings can be saved and loaded back using the **Save To** and **Load From** buttons at the bottom of the window. You can choose to save or load settings to either the cellview, library of the cellview, technology of the cellview, or a specified file. If you are saving to a file, the settings from both the *Layout Editor Options* and *Display Options* windows will be saved. Click **OK** when done.
- Back in the layout window, select **Options** → **Layout Editor**. The *Layout Editor Option* window will appear. Options here allow you to change the editing commands of the editor and change how the cursor behaves.

- In the *Layout Editor Option* window, uncheck the **Gravity On** box. This will prevent the cursor from being attracted to other objects already drawn in the cellview. Experiment on your own. If you feel that you are comfortable with this function or find it useful in certain situations, you can turn it on. Click **OK** when done.

3.2 Layer Selection Window (LSW)

The *Layer Selection Window (LSW)* lets you to choose the layer on which you create objects (called the entry layer). It also controls which layers are selectable or visible.

- To change the LSW to make the layers selectable or visible, move the cursor over the layer and click using the middle button. It will toggle layer visibility and also automatically makes invisible layers not selectable. The text layer color disappears to show the layer is invisible. The layer name turns gray to show the layer is not selectable.
- Every time after you have selected a layer, select **Window** → **Redraw** to see the effect of any LSW changes you have made. This will allow you to make several changes in the LSW before taking time to redraw the cellview, especially in complex designs.
- To make the layers visible, click on the **AV** (All visible) button. The colored squares showing the layer color reappear, and the shading on the layer name disappears.
- Use the left mouse button to select layers for entry in the LSW. The abbreviation dg after each layer name means drawing.
- For drawing active regions, we select the **oxide** layer in LSW.
- **Pimp** layer represents pplus and **Nimp** layer represents nplus.
- Contact loses is **Cont**.



If the layers in LSW display the same color, you need the **display.drf** file. The file **display.drf** can be found in *packages/cadence/cells/generic/gpdk_MIET_2.0*. copy this file to your Cadence running directory using the following command and exit and run icfb again:

```
cp /packages/cadence/cells/generic/gpdk_MIET_2.0/display.drf ./
```


3.3 Creating Shapes and Objects

Most of the layers that you will draw will be rectangles or polygons that are rectilinear in shape. The sizes of the objects depend on the design and the design rules.

3.3.1 Creating rectangles

- To create rectangles, select a layer from the LSW, then select **Create** → **Rectangle** or click on the **Rectangle icon** on the left. In the new window that appears, type the net name you want the rectangle to be associated with. You can choose to leave it blank and name the net later.
- Note that assigning names to the nets aid in the future layout verification processes. However, ensure that the net names on the layout matches that ones in the schematic, otherwise the LVS program (refer to section 4.3) will fail to match nets.

3.3.2 Creating Polygons

- Another way creating objects is to create polygons. Select a layer from the LSW, then select **Create** → **Polygon** or click the **Polygon icon** on the left. In the new window that appears, type the net name you want the polygon to be associated with. You can choose to leave it blank and name the net later. Set Snap Mode to Orthogonal. The snap mode controls the way segments snap to the drawing grid as you create the polygon by placing its vertices.
- Point and click on the first point of the polygon. The CIW will prompt for the second point of the polygon. Move the cursor to click on a second point. The layout editor will create a solid line parallel to either the Y-axis or the X-axis. Continue to click on a third point that is orthogonal to the solid line. The layout editor will create two solid lines at right angles to each other between the points you entered. You will also see two dashed lines at right angles to each other between the points you entered. The dashed lines show how the layout editor would finish the polygon if you click twice on this point you entered.
- If you have made a mistake in one of the points while creating a polygon, you can hit the *Backspace* key to undo them.

3.3.3 Creating Pins

- To create pins, select **Create** → **Pin**. In a window that appears, change the *Mode* to *shape pin*. A new window named Create Shape Pin will replace the previous window.
- Enter the pin net name in the *Terminal Names* field. Make sure that the names exactly match the schematic (case sensitive). If you are not sure about the names of the pin nets, open the schematic and check the net properties.
- Turn on the *Display Pin Name* option if you would like the pin names to be displayed on the layout cellview. Click the *Display Pin Name Option* button to change the display properties of the pin names.
- Select the I/O type accordingly. For power and ground pins, select *inputoutput*.
- Move the cursor to where you want to place the pin and click.

3.4 Selecting Objects for Edit

To edit an object, first you need to select it. There are two selection modes: full and partial. Press the F4 key to toggle between the modes and the mode is displayed in the status banner of the layout window (top).

3.4.1 Selecting Objects

- To select an object, set the selection mode and click
- To deselect all objects, click in an empty part of the design.
- To select one or several objects at a time, press the Shift key while selecting.
- To deselect one or several objects after they have been selected, press the Ctrl key and select.

3.4.2 Editing Objects

There are several functions that are often used to edit objects. They include: move, copy, delete, stretch and merge. Should you require more advanced editing methods, please refer to the Editing Objects section in the Virtuoso Layout Editor User Guide.

3.4.3 Moving Objects

- To move the object, you can select **Edit** → **Move** from the drop down menu or use the **Move icon** on the left. The Move window appears. After you have selected the object, the CIW will prompt you for a reference point for the move. Click on the reference point for the move, and drag the pointer to the destination point. The object will be moved with respect to the reference point.
- Note that in the Move window, there is a Change To Layer option. This will allow you to move and change the object from one layer to another without having to redraw the object. Check the box to enable the Change To Layer function and move the object as usual.
- You can rotate or flip the object (sideways or upside down) by clicking the Rotate, Sideways and Upside Down buttons in the Move window before placing the object.

3.4.4 Copying Objects

- To copy an object, select **Edit** → **Copy** or use the **copy icon** after you have selected the object. After the copy window appears, select the object to be copied. The CIW will ask you for a reference point (start point) for the copy. Click on the reference point for the copy and drag the pointer to the destination point. The object will be copied with respect to the reference point.
- To copy and paste multiple copies of the object, type in the number of copies in either the Rows or Columns fields and place the objects in the cellview as usual.
- Note that in the Copy window, there is Change To Layer option. This will allow you to copy and change the object from one layer to another without having to redraw the object. Check the box to enable the Change To Layer function and copy the object as usual.
- You can rotate or flip the object (sideways or upside down) by clicking the Rotate, Sideways and Upside Down buttons in the Copy window before placing the object

3.4.5 Deleting Objects

- To delete an object, select **Edit** → **Delete** or press **delete key**.

3.4.6 Stretching Objects

- To stretch an object, select **Edit** → **Stretch** from the drop down menu or use the **Stretch icon** on the left. Click on the reference point for the stretch and drag it to

the destination point. The object will be stretched with respect to the reference point.

3.4.7 Merging Objects

- You can use the merge function to merge two objects of the same layer. To merge objects, select the objects to be merged, then select **Edit** → **Merge**.

3.4.8 Saving the Design

- To save the design, select **Design** → **Save** or click on the **Save icon** on the left.

4.0 Layout Verification

After you have completed the layout, you need to perform layout verification to ensure that the layout does not violate any design rules.

4.1 Design Rule Check (DRC)

DRC checks your layout against physical design rules defined in the **divaDRC.rul** file. It will display error information if it finds any part in the layout that violates the design rules. Note that this is only a physical design check and does not verify the actual performance or functionality of the layout design.

- To run DRC, select **Verify** → **DRC** from the drop down menu. Check the Rules File and the Rules Library fields are correct in the DRC window. Click OK to start.
- If there are any errors, it will be reported in the CIW. A blinking polygon, called an error marker, appears in the cellview at the location of the error.
- To view the errors and get a brief description of the error, select **Markers** → **Explain** and click on the error marker. The marker will be highlighted indicating it is selected. A window named marker test will appear that contains information about the cellview that contains the error and the rule is violated.
- To quit the Explain command, press the *Esc* key.
- To remove the markers, select **Verify** → **Markers** → **Delete All**. The Delete All Markers window appears. Click OK to remove the Markers.
- If any errors are reported, make changes to the layout and re-run the DRC until all errors are fixed.

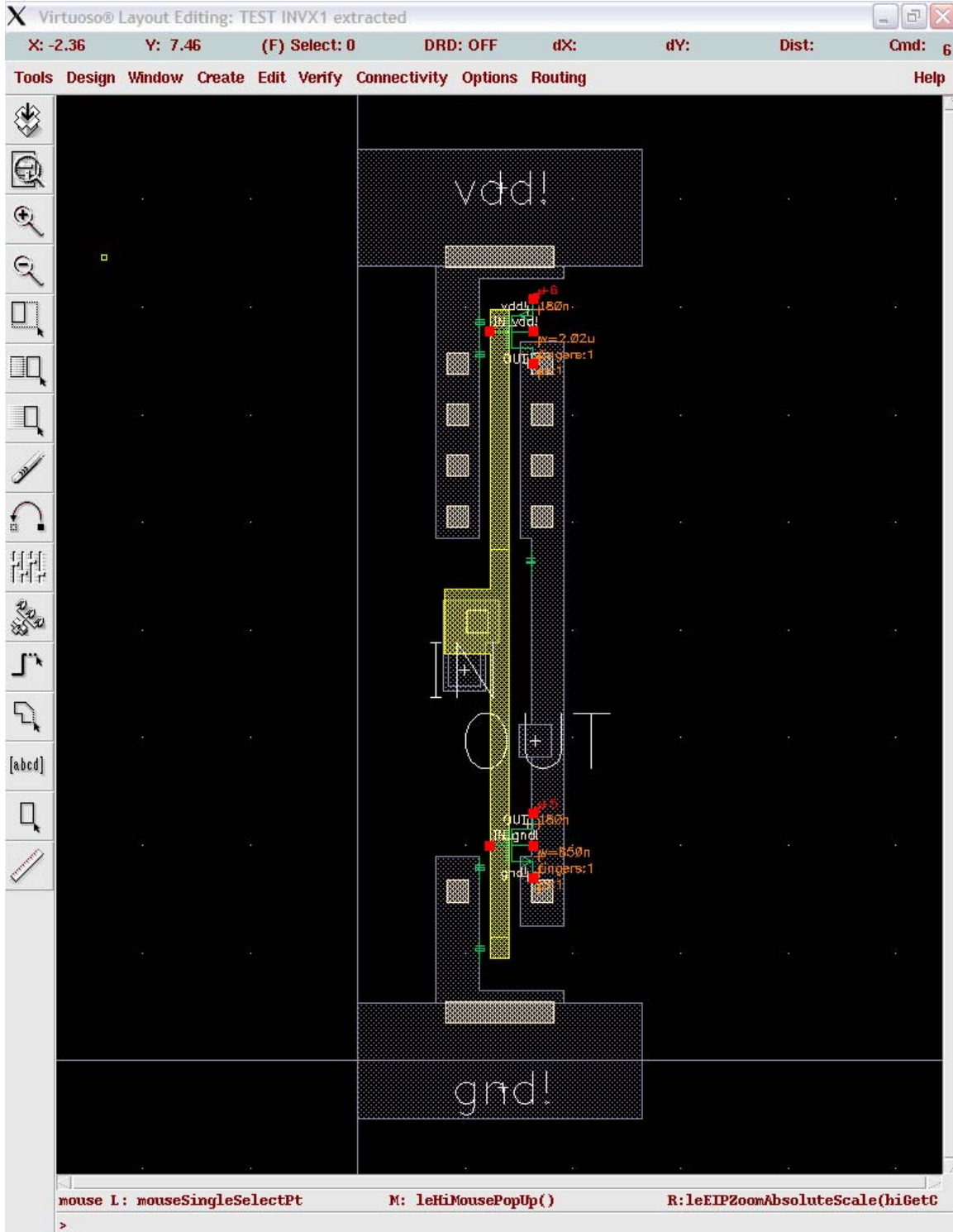
- For large complex designs, it is better to run an incremental DRC. This means that the system will keep track of any changes you have made since the last DRC and it will check only the changes made. This will make DRC run faster as it does not have to check every part of the design.
- To turn on the incremental DRC, set the **checking limit** to **incremental** in the DRC window.

4.2 Connectivity Extraction

Before performing a Layout Versus Schematic (LVS) check, you need to extract the connectivity from the layout cellview by running the Extract program. The Extract program uses rules defined in the **divaEXT.rul** file to recognize devices and establish electrical connections or nets. It will create an extracted cellview that shows the nets.

- To run the Extract program, select **Verify** → **Extract**.
- In the *Extractor* window, select **flat** as the *Extract method*. A flat extract method is used because parasitic capacitance values can vary between different instances of the same cell, thus each cell must be extracted.
- Turn on *Join Nets with Same Name*. This will merge nets with the same names while suppressing warning messages about different nets that have the same name.
- To select the types of parasitics that are to be extracted, click the **Set Switches** button in the *Extractor* window. In the *Set Switches* window that appears, select the type of parasitics that are to be extracted (typically parasitic capacitances). Click **OK** when done selecting.
- Click **OK** or **Apply** in the *Extractor* window to create the extracted views.
- The extraction rules appear in the CIW as the extract program executes. When the extraction is complete, a message saying that the extracted cellview is saved will be shown.
- To view the extracted cellview, select **File** → **Open** from the CIW. It should be under the same library and cell name. Select the extracted view name and click **OK**.
- The extracted cellview appears on top of the layout cellview. Notice that the extracted cellview is similar to the layout, but the gates now have symbols at one end. Displayed next to the symbols are the gate width and length.
- To display the electrical connections, open the *Display Options* window and select *Nets*. Click **Apply** when done.

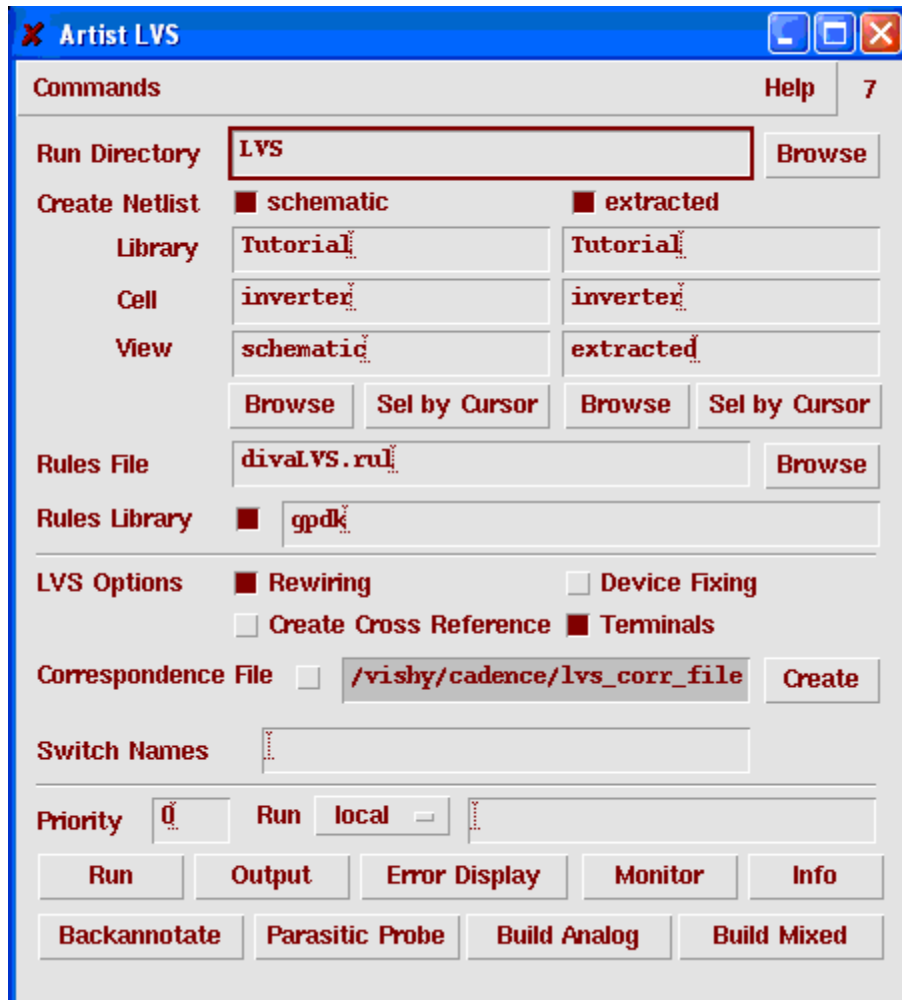
Extracted View



4.3 Layout Versus Schematic (LVS) Software.

As the name implies, the LVS program performs a comparison of the schematic to the physical layout. It will use both the extracted view and the schematic view of the layout. If you did not create an extracted view, LVS will not work.

- To run LVS, select **Verify** → **LVS**
- If a *LVS Form Contents Different* window appears, click **OK** to continue.
- In the LVS window, fill in the schematic and extracted fields either with **Browse** or **Sel by Cursor** button. If you choose to use the **Sel by Cursor** button, click on the button, and then simply click in any area of the schematic or extracted cellview window.
- Note that if both the schematic and extracted cellview are opened before the LVS window, the fields should already be fitted automatically. Check to ensure that they are correct.
- Make sure that specified Rules File is **divaLVS.rul** and Rules Library is **gpdk**.
- Turn off the *Correspondence File* option. The purpose of the correspondence file is to allow the user to identify schematic/layout nodes that should be mapped to each other. Mainly you would do this if LVS has trouble matching the schematic and layout on its own.



- Click **Run** to start LVS. When the save cellview window appears, click **OK** to save. The LVS job runs in the background and might take a couple of minutes to complete, depending on the complexity of the design. When the job is finished, a dialog box named *Analysis Job Succeeded* will appear. Note that this only means that the LVS program was executed successfully and does not mean that the layout matches the schematic.
- To view the LVS results, click **Output** in the LVS window. A text window listing the output from the LVS run appears. Scroll down until the section that compares the layout and the schematic is displayed. In that section, it will report whether the two designs match and provide a list of the numbers if instances and nets.

If LVS verifies that the layout matches schematic, it will report:

The net-lists match

Otherwise, it will report:

The net-lists failed to match

- If the layout fails to match the schematic, the errors on the layout must be corrected.

```
o(#)$CDS: LVS.exe version 5.1.0 09/27/2005 22:43 (cicln01) $
Command line: /packages/cadence/ic5141/tools/dfl/bin/32bit/LVS.exe -dir /home/vishy/cadence/LVS -l -s -t /home/vishy/cadence/LVS/layout /home/vishy/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

GENERIC PDK LVS Rules

Net-list summary for /home/vishy/cadence/LVS/layout/netlist
count
4      nets
3      terminals
1      pmos
1      nmos

Net-list summary for /home/vishy/cadence/LVS/schematic/netlist
count
4      nets
4      terminals
1      pmos
1      nmos

Terminal correspondence points
N2      N4      IN
N1      N2      OUT

Devices in the rules but not in the netlist:
mplusres polyres nmoscap mincap vmpm rpm pmp inductor ndio pdio

The net-lists match.

          layout schematic
          instances
un-matched 0      0
revised    0      0
size errors 0      0
pruned     0      0
active     2      2
total      2      2

          nets
un-matched 0      0
merged     0      0
pruned     0      0
active     4      4
total      4      4
```

4.4 Displaying the Errors

- Make sure that the extracted cellview is opened before you continue.
- To display the errors, click the **Error Display** button at the bottom of the LVS window.
- In the LVS *Error Display* window that appears, click the **First** button in the *Display* field. The error messages will be displayed below the *Display* field. In addition, the geometries in the extracted layout that do not match anything in the schematic will be highlighted in the color specified in the *Error Color* field.
- To clear the markers, click on the **Clear Display** button in the LVS *Error Display* window.
- If the layout matches the schematic, a netlist can be extracted from the layout to examine the performance of the design. Otherwise, errors on the layout must be corrected, followed by a DRC run on the corrected layout, a re-extraction of the layout and a LVS run. Repeat until that final layout matches the schematic.

4.5 Probing the Schematic and Layout

If the layout fails to match the schematic, probing can be used to aid in finding the error. Note that this is just a tool to aid in the troubleshooting process and does not automatically locate or fix the errors.

- To probe a design, click the **Probe Form** button in the *LVS Error Display* window.
- Make sure that the schematic cellview cellview is opened before you continue (for cross probing).
- In the Probing window that appears, change *Probing Method* to cross probe and click on the **Add Device** or **Net** button.
- Point to a device or net in either the extracted or schematic cellview. The corresponding device or net that LVS has compared with will be highlighted in the other cellview. Alternatively, enter the name of the device or net in quotes in the CIW and they will be highlighted in both cellviews.
- A single probe can be performed in a similar fashion by selecting the *Probing Method of single probe*. This is useful in locating the errors when given a device or net name LVS.
- To remove the markers, click on the **Remove All** button in the *Probing* window.